REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1 and 3-17 are presently active in this case. Claims 1, 3, 9, and 14 have been amended by way of the present amendment.

In the outstanding Office Action, Claims 1, 3, and 4 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,208,170 to Iwaki et al; Claims 8-10 were rejected under 35 U.S.C. § 102(b) as anticipated by Japanese Patent Publication No. 6-29834; and Claims 14 and 16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Iwaki et al. in view of Japanese Patent Publication No. 6-29834.

Claims 5-7, 11-13, 15, and 17 were indicated as being allowable. Applicants acknowledge with appreciation the indication of allowable subject matter.

Applicants further acknowledge with appreciation the courtesy of an interview granted to Applicant's attorney on July 15, 2003 at which time the outstanding rejections were discussed in view of Applicant's proposed claim changes. It was agreed during the interview that claim 1 was allowable as amended in the proposed claims. No agreement was reached with regard to claims 3, 4, and 14. Finally, Examiner Tan indicated that claims 8-10 and 16 would be reconsidered upon the submission of a formal response.

Regarding the rejection of claims 3, 4, and 14, Applicants point out that those claims define a second transistor connected between the second reference voltage line and the virtual voltage line, and which is provided for every two or more gate circuits. Because of this configuration, testing can be readily performed for each gate circuit, and it is possible to separately switch operations of each gate circuit at high speed.

In contradistinction thereto, because Iwaki discloses a configuration where a transistor is shared with a plurality of low Vth logic circuits, it is not easy to perform testing of each

low Vth logic circuit. Hence, Iwaki is not believed to anticipate or render obvious the subject matter of claims 3, 4, and 14.

Regarding the rejection of claims 8-10 and 16, Applicants point out that those claims define a storage circuit capable of holding output logic of the gate circuit. The storage circuit includes transistors with a high threshold voltage.

In contradistinction thereto, Fig. 6 of Japanese Patent Laid-open Pub. 29834/1994 discloses a high threshold logic circuit 30 including transistors with high threshold value, and a low threshold logic circuit 20 which supplies the clock to the circuit 30. The official action asserts that the low threshold logic circuit 20 corresponds to the gate circuit. However, Applicants submit that the low threshold logic circuit 20 supplies only the clock to the high threshold logic circuit 30, and the circuit 20 does not supply data to be latched to the high threshold logic circuit. Consequently, the low threshold logic circuit 20 has a function completely different from that of the gate circuit of the present invention which supplies data to be latched to the storage circuit. Thus, the circuit disclosed in Fig. 6 of Japanese Patent Laid-open Pub. 29834/1994 has a circuit configuration completely different from that of the circuit of claims 8-10 and 16 and therefore is not believed to anticipate or render obvious the subject matter defined thereby.

Consequently, in view of the present amendment, no further issues are believed to be outstanding in the present application, and the present application is believed to be in condition for formal allowance. An early and favorable action is therefore respectfully requested.

Respectfully submitted,

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